

## ABSTRACT OF THE DISCLOSURE

A master DLL circuit (3) generates a first delay signal (CKD) by delaying the master clock signal by a first delay time (T0) and generates a first pulse signal (Smp) having a pulse width (T0) of the first delay time, and generates a first control signal (Scp) which is changed in accordance with the first pulse signal (Smp), and adjusts the first delay time (T0) in accordance with the first control signal (Scp). Each slave DLL circuit (D1 to Dm) delays, by a second delay time (td), a delay internal clock signal, and outputs the delayed delay internal clock signals (CK1 to CKm) which form the multiphase clock signals. Each slave DLL circuit generates a second pulse signal (Ssp) having a pulse width (td) of the second delay time, and generates a second control signal (Scp1) which is changed in accordance with the first and second pulse signals (Smp, Ssp), and adjusts the second delay time (td) in accordance with the second control signal (Scp1), thus reducing a skew value of the multiphase clock signal.